



Samsung Memory Solution for HPC

- The leverage of right choice of DRAM in improving performance and reducing power consumption of HPC systems -

8. September 2011

Samsung Semiconductor Europe GmbH

Gerd Schauss

Marketing Intelligence

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Samsung, WW#1 Total Memory Solution Provider

SAMSUNG

'92 '93 '95 ... '01 ... '06 '07 '08 '09 '10

MEMORY

DRAM

NAND

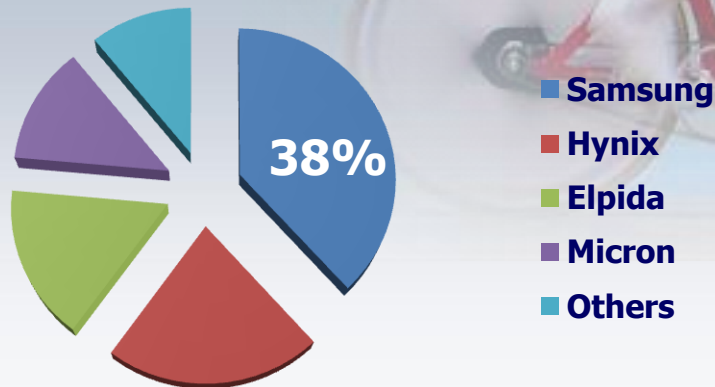


for 18 years

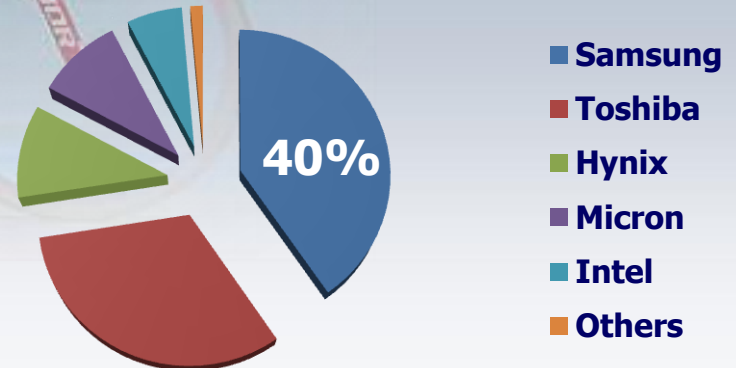
for 19 years

for 10 years

DRAM market share ('10)



NAND market share ('10)



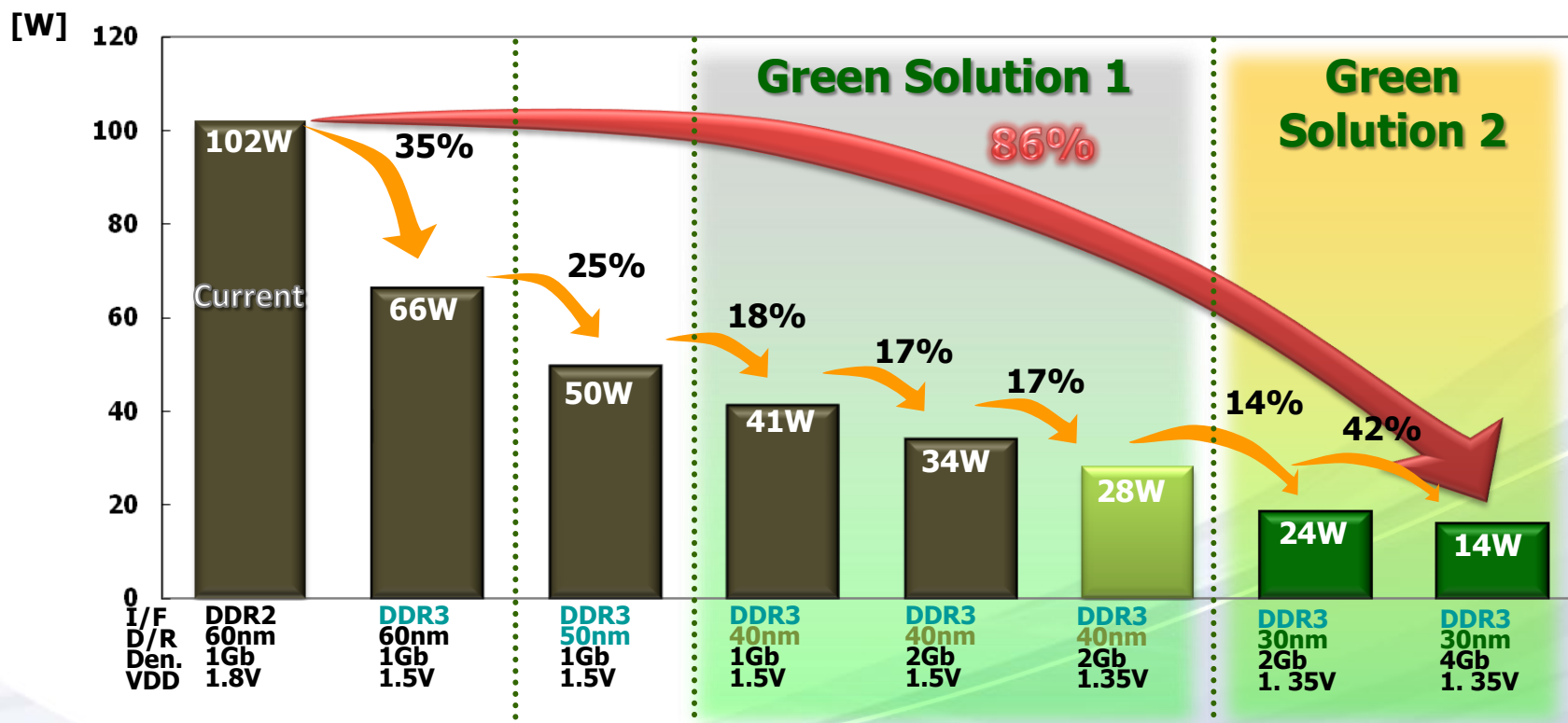
SAMSUNG Green Memory Solutions

SAMSUNG



Source: SAMSUNG

- **SAMSUNG Green solution can save about 86% of Power consumption against DDR2 solution**

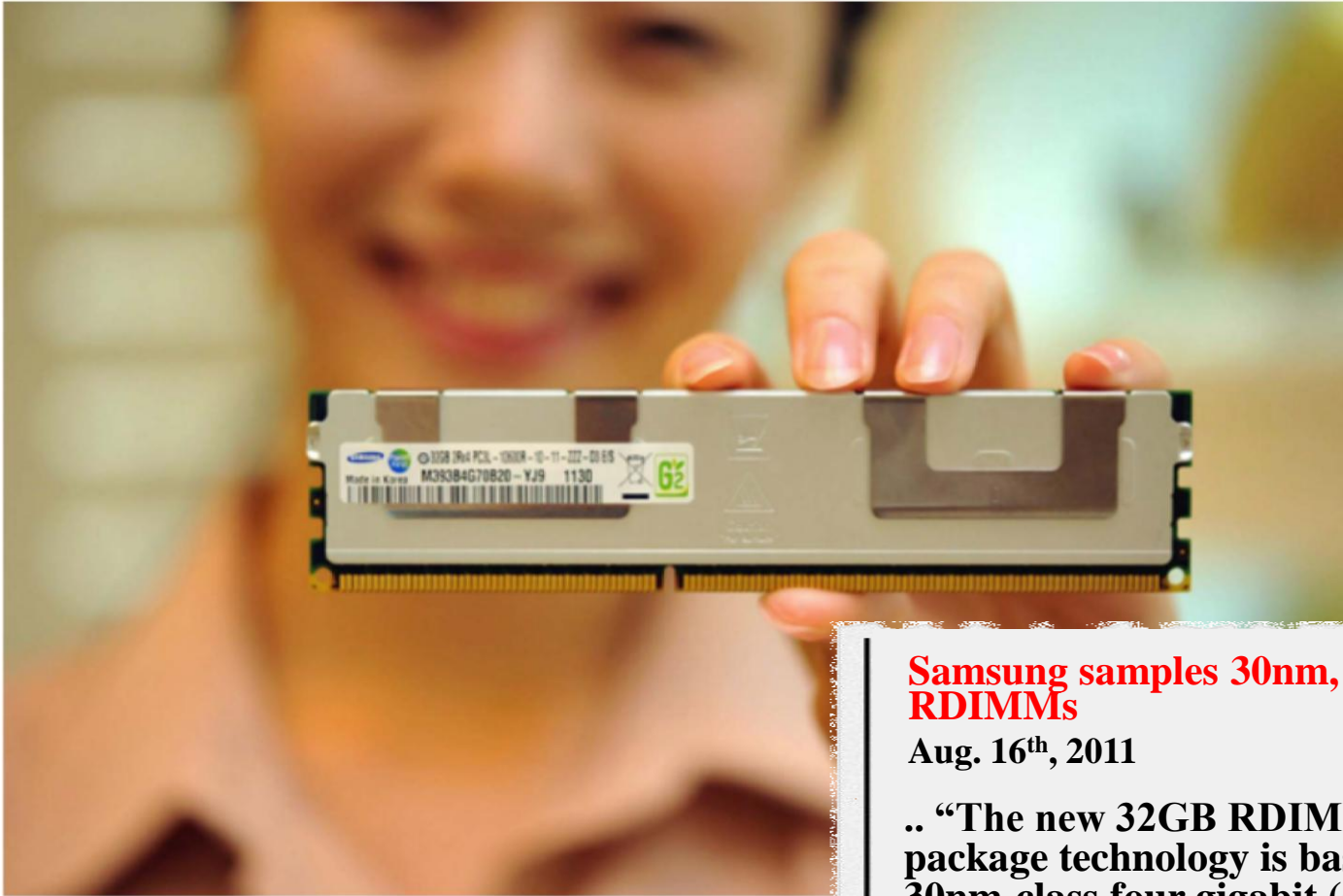


■ Considered the 8hours active and 16hours idle status in server

Source: Measured by Samsung Lab.

Samsung announced 32GB with TSV technology

SAMSUNG



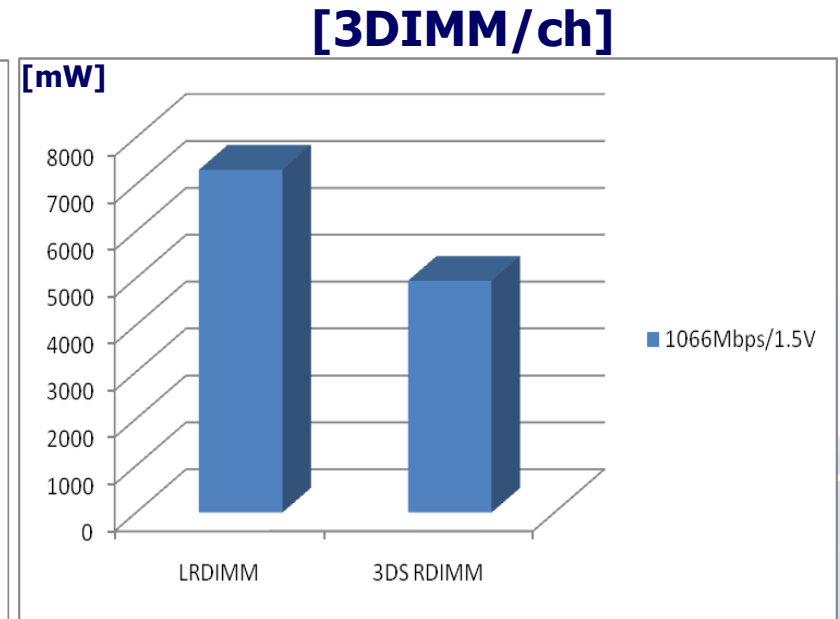
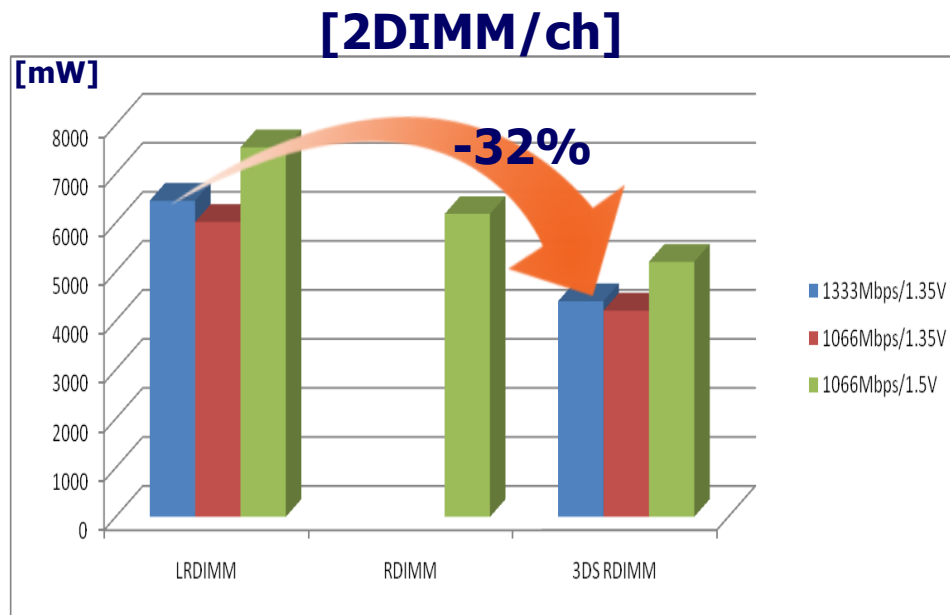
Samsung samples 30nm, 32GB DDR3 RDIMMs

Aug. 16th, 2011

.. “The new 32GB RDIMM with 3D TSV package technology is based on Samsung's 30nm-class four gigabit (Gb) DDR3. It can transmit at speeds of up to 1,333 megabits per second (Mbps), a 70 percent gain over preceding quad-rank 32GB RDIMMs with operational speeds of 800Mbps.”...

32GB TSV RDIMM Power Evaluation Results

■ TSV RDIMM shows -32% power decrease over LRDIMM@1333



Common condition : 32GB (based on 30nm 4Gb), RST-Jump
- RDIMM : RC AB, 2RCD
- 3DS RDIMM : RC AB based, 2RCD

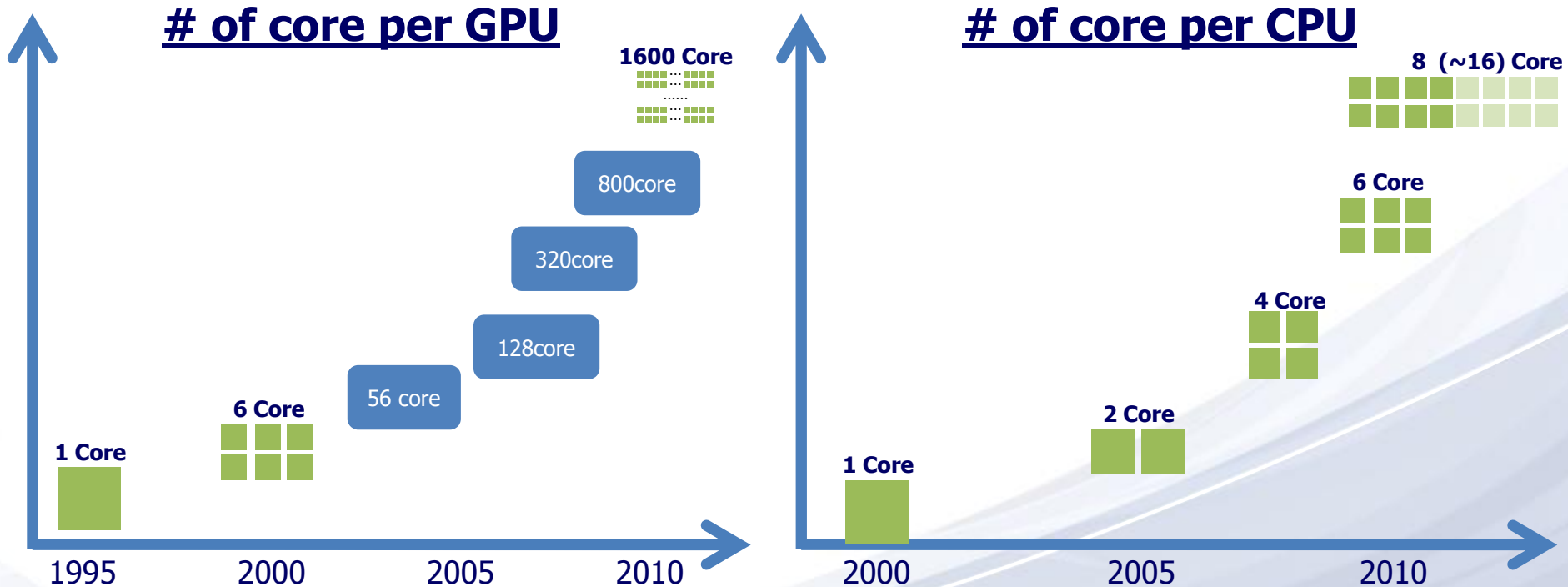
Successfully developed POC in Current System

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Memory Performance Requirement Keeps Growing

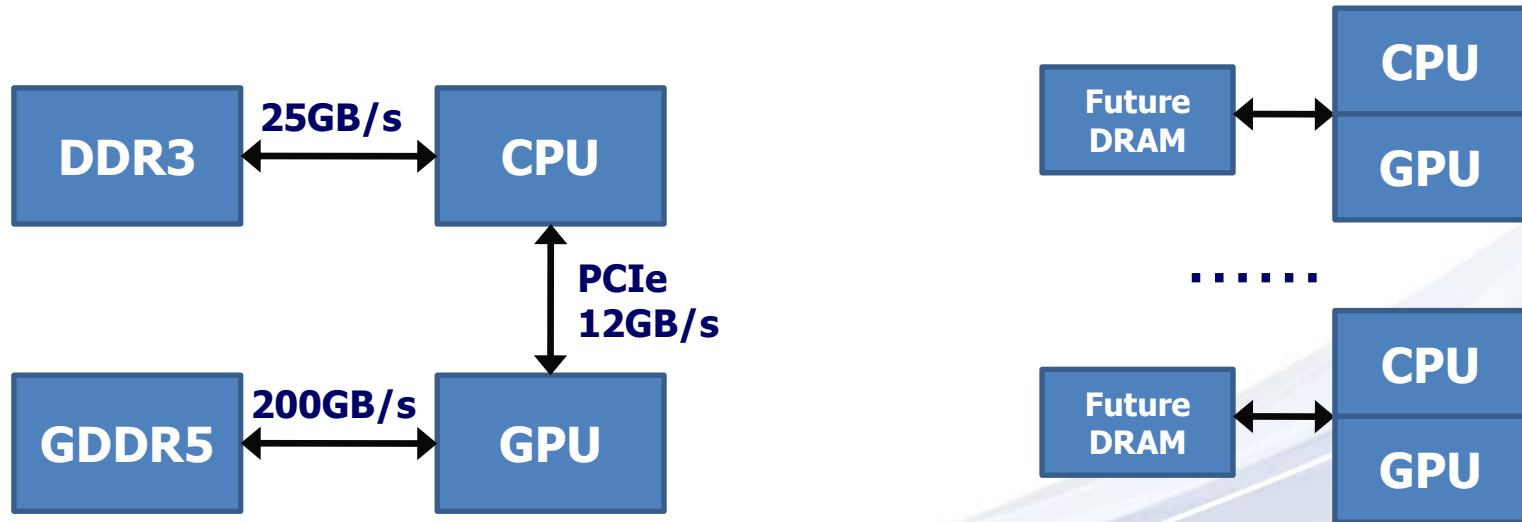
- # of processor core and performance keeps growing
- CPU + GPU heterogeneous computing needs more fast DRAM
- Memory bandwidth should increase to hide data I/O time



Last 10 years, # of GPU core increased by 260X and # of CPU core by 8X

Memory Performance Requirement Keeps Growing

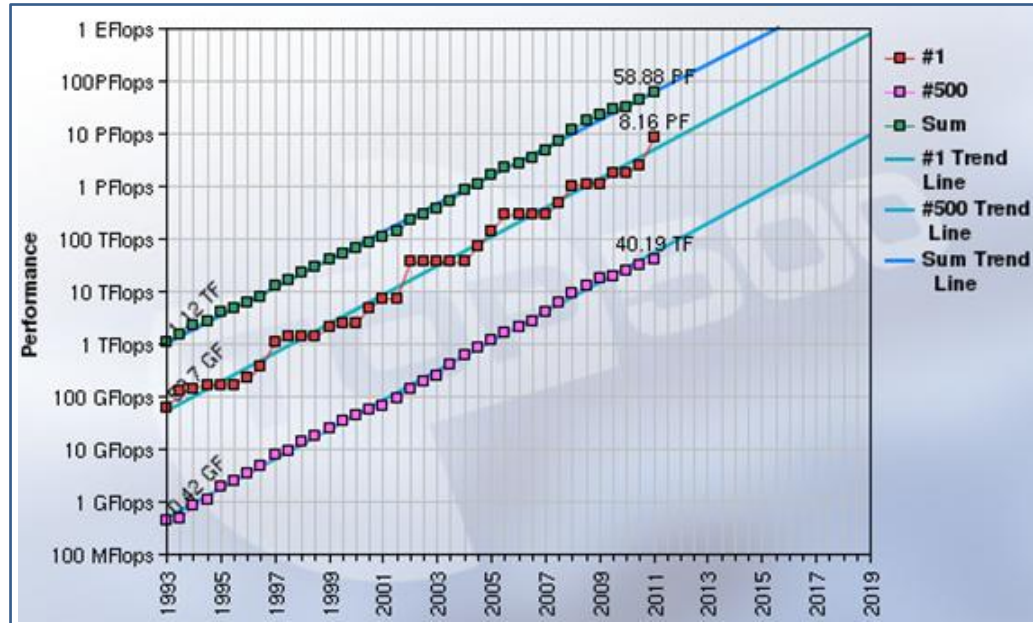
- # of processor core and performance keeps growing
- **CPU + GPU heterogeneous computing needs more fast DRAM**
 - In current heterogeneous, data motion thru PCIe is bottleneck
 - Strong movement to go towards On-die heterogeneous
- Memory bandwidth should increase to hide data I/O time



Current Heterogeneous Computing

Future Heterogeneous Computing

- The world is heading forward for exascale computing realized until 2018



*Source: top500.org

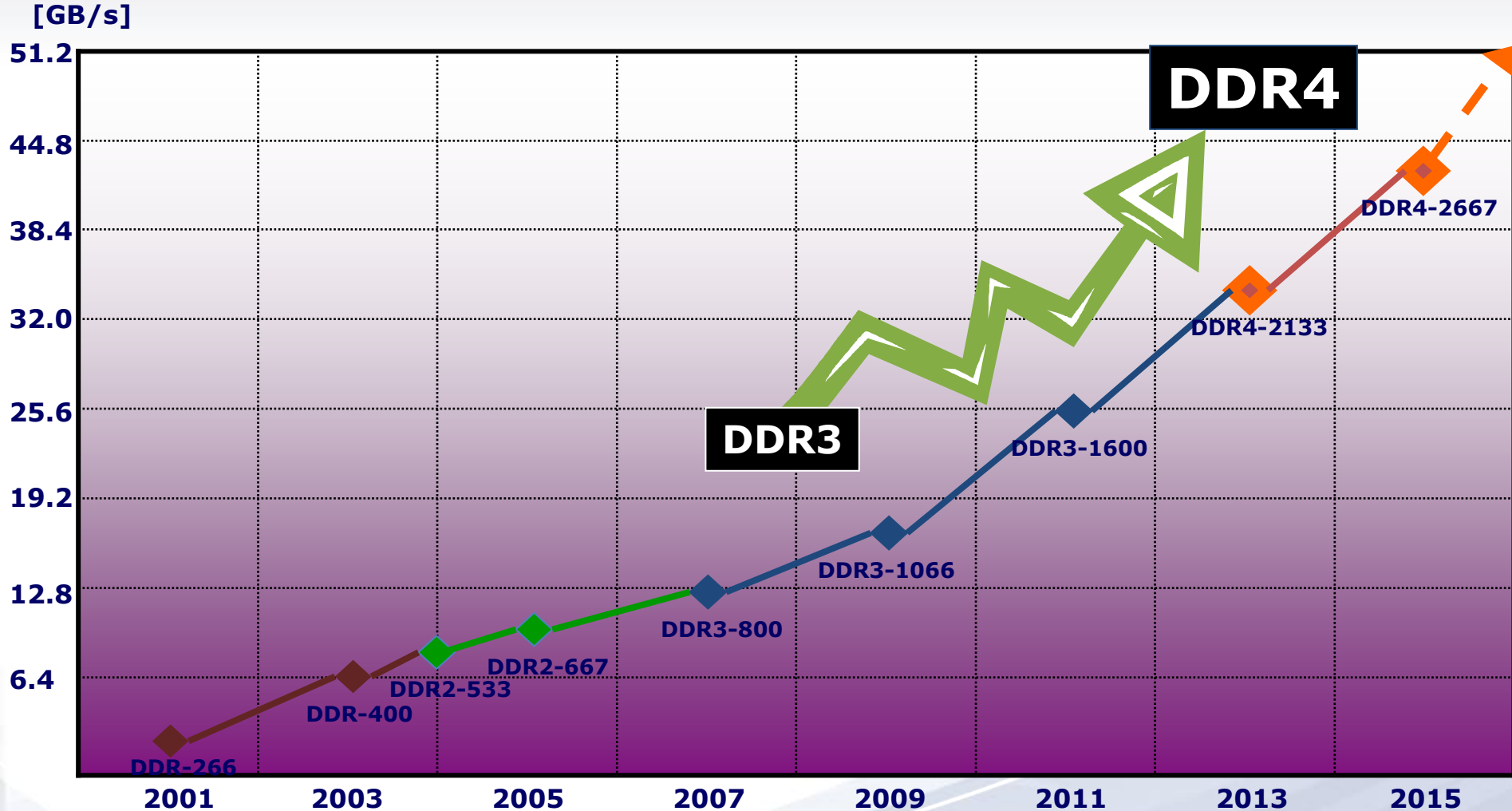
- **10X Performance/Watt is needed compared to current computing**
 - Future computing: $\sim 20\text{pJ/Flop(DPFP)}$
 - $20\text{pJ/Flop} \rightarrow 50\text{GFLOP/W} \rightarrow 10\text{TFLOP/200W} \rightarrow 1\text{EFLOP/20MW}$ (US/EU directive)
 - Current computing: $\sim 200\text{pJ/FLOP(DPFP)}$ K-Computer ($\sim 1.000\text{pJ/FLOP}$)

Not just performance, but performance / watt is important for exascale

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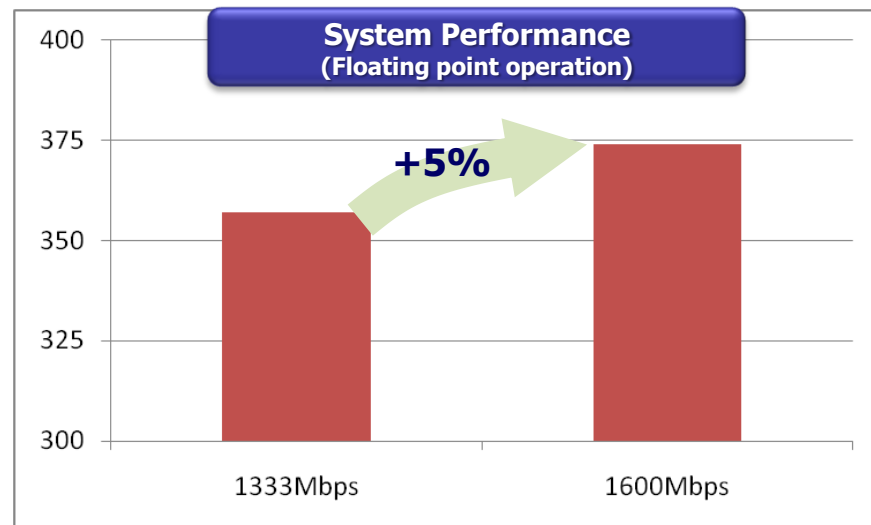
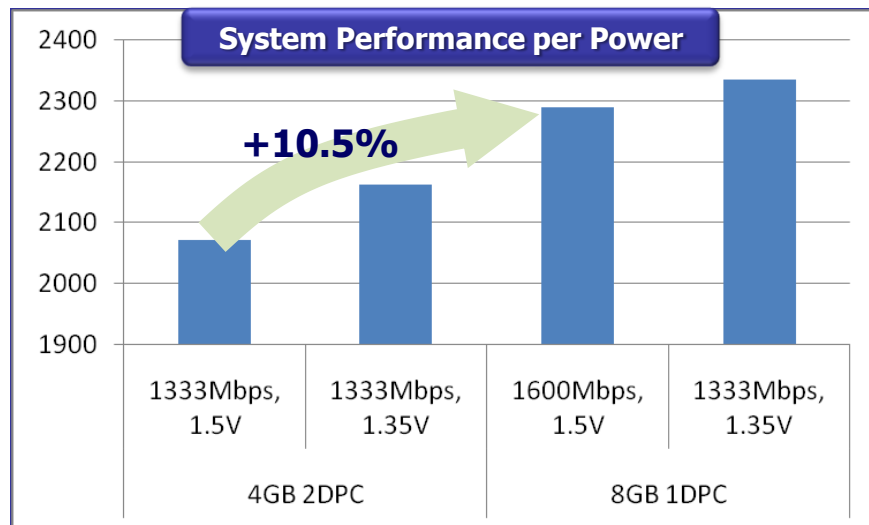
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DDR4 Will Keep Performance Increase Trend



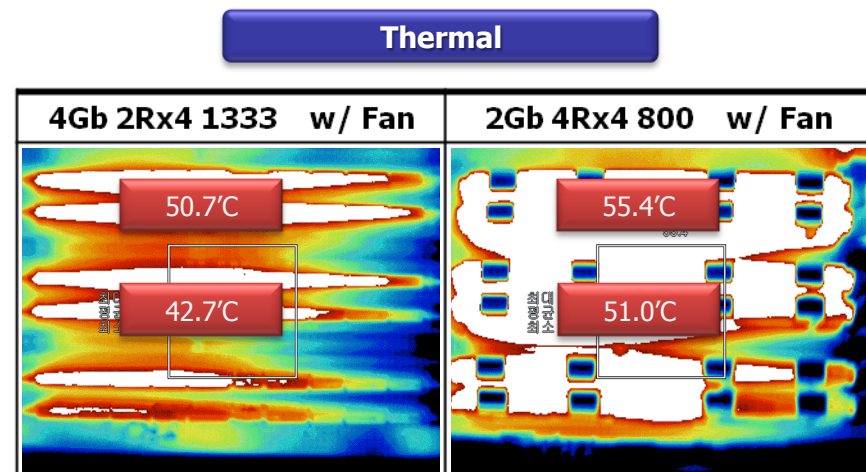
Double bandwidth over DDR3

■ High-density & High-speed memory increases system's value



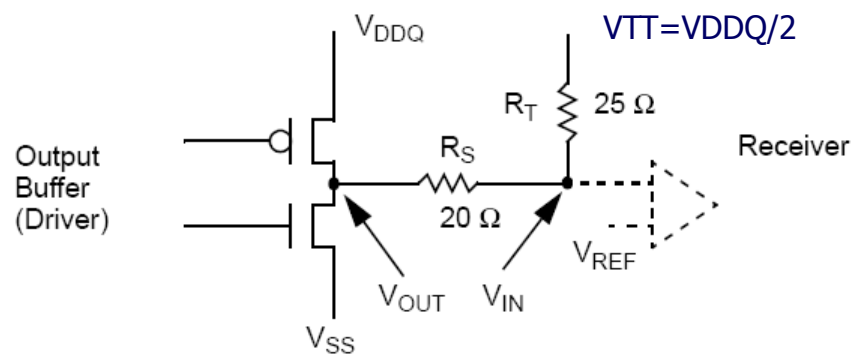
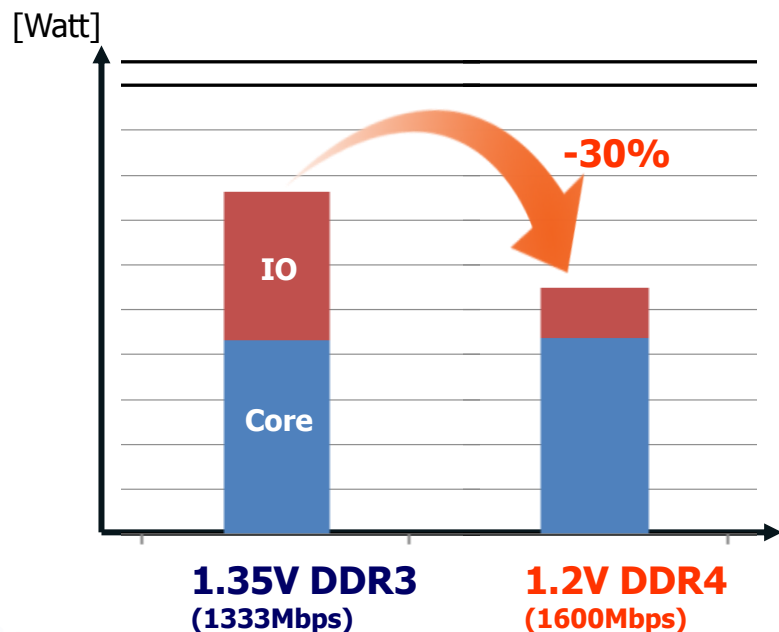
■ High-density component with less # of DPC is better

- Better system performance
- Better performance per power
- Better thermal environment



■ Key value of DDR4 is efficient power with high performance

- Adopted many power saving & fast power-down exit features
- Saved IO power with POD interface: Suit for high speed



SSTL (DDR3)



How Samsung Keeps Innovation for Green Memory

- Samsung has been the leader of keeping innovation for higher density with less power

Samsung Trumpets Green 30nm DRAM

February 1st, 2010
www.softpedia.com

.. "most advanced low-power DDR3 available today"...

Samsung to Make DDR3 Memory Using 30nm Process Technology

February 1st, 2010 01:30 PM
www.Xbitslab.com

.. The 30nm-class process when applied to DDR3 mass production raises productivity by 60% over 40nm-class DDR3 and reduces power consumption by up to 30% compared to 50nm-class DRAM ..

Samsung starts mass production of 2Gb DDR3 DRAM using 30nm tech

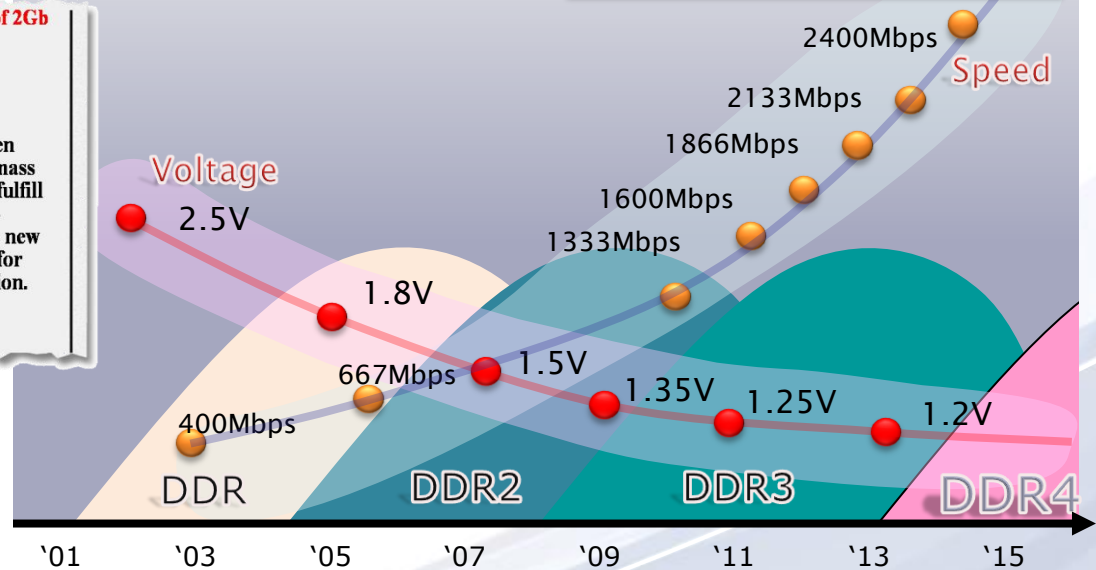
July 21st, 2010

.. "Announced earlier this year, Samsung's 30nm-class 2Gb Green DDR3 DRAM has now entered mass production and will be ready to fulfill the need for faster, more energy-efficient memory sparked by the new generation of servers optimized for cloud computing and virtualization."

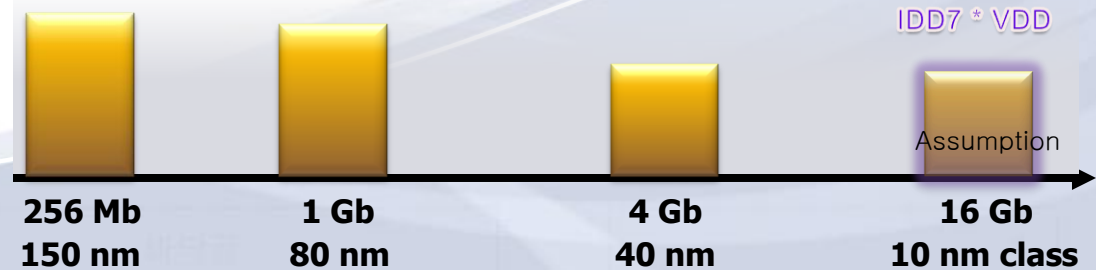
..."



High speed at low voltage



High capacity with low power

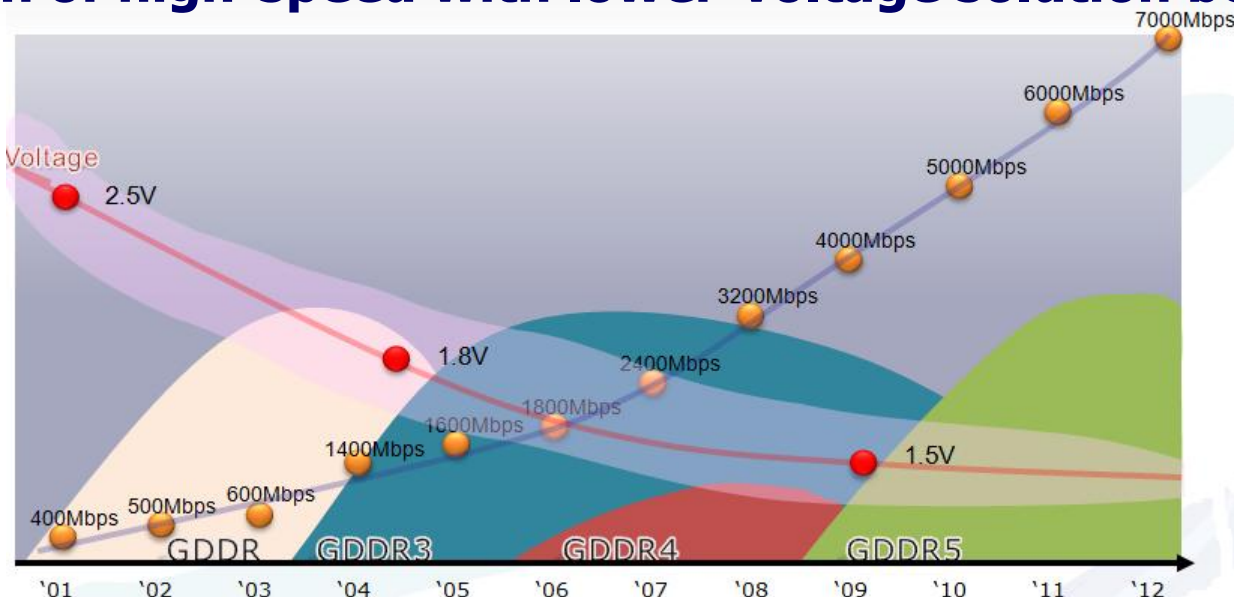


IDD7 * VDD

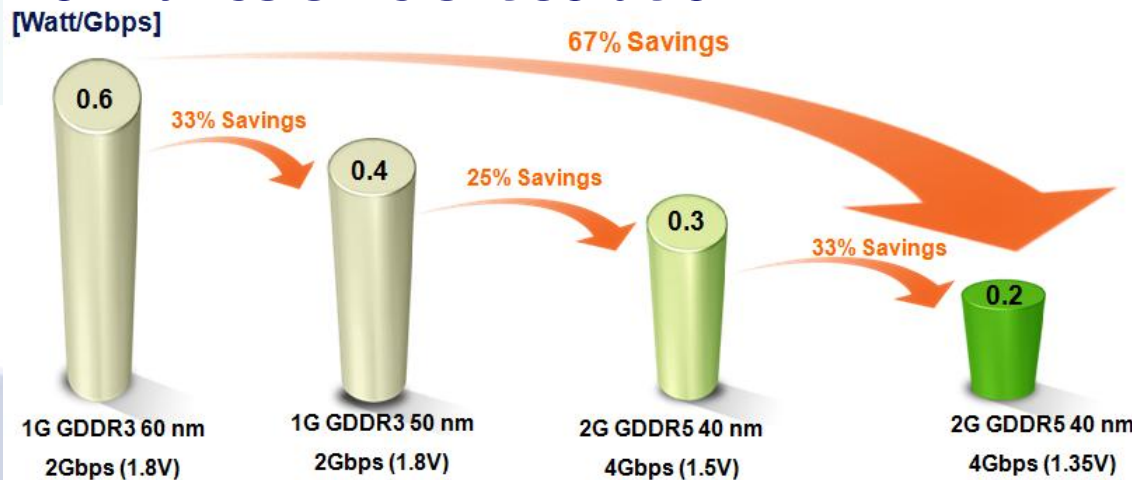
Assumption

GFX DRAM for Heterogeneous Computing Keeps Evolving

■ Evolution of high-speed with lower-voltage solution been kept



■ DRAM process & design improvement realized much more power/performance efficient solution



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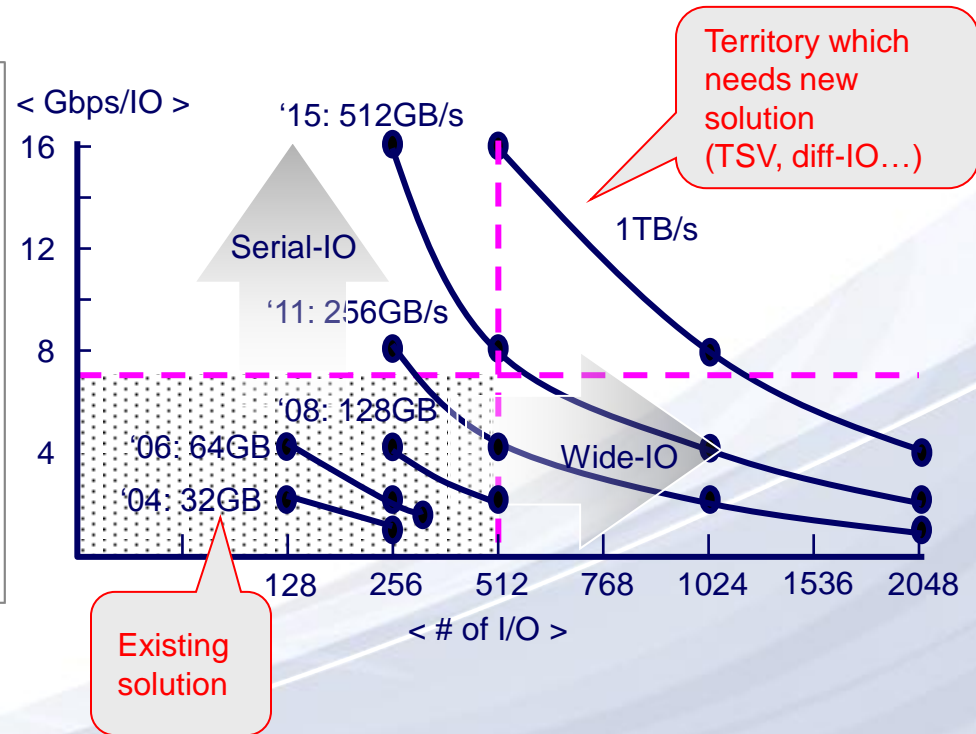
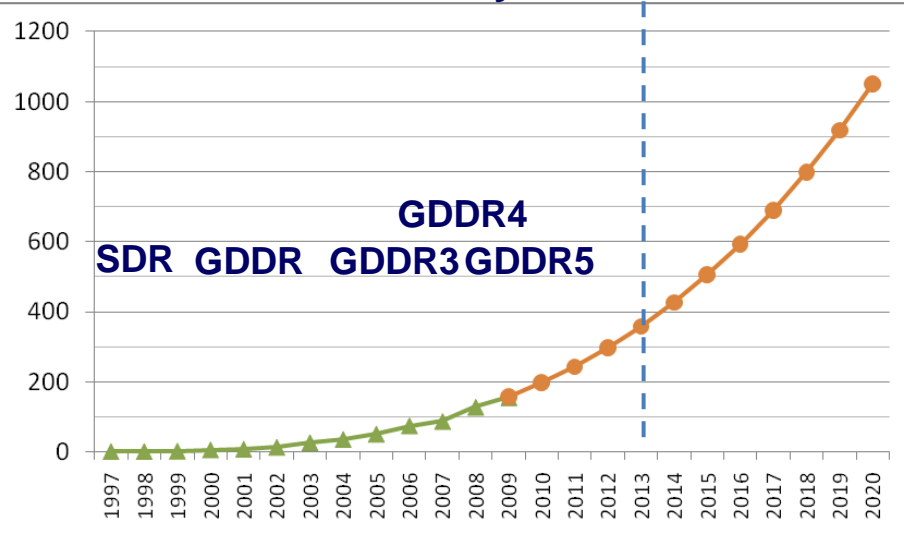
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New High-performance Memory is Getting Needed

■ GPU performance keeps increasing and GFX memory performance requirement keeps growing

- Current solution's limit: 7Gbps(GDDR5) X 512 IO's = 448GB/s

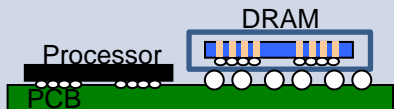
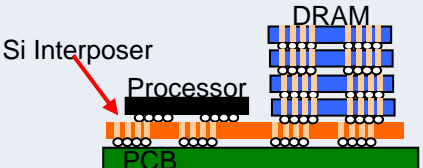
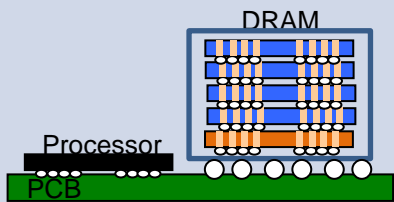
GFX card memory BW trend



Consideration for Next High-performance Memory

■ Several solutions can be considered

- To meet performance requirement within power budget for Exa-scale

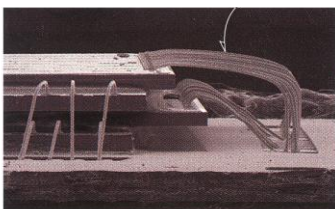
	BW per DRAM pkg	Memory BW per Processor	System configuration	Watt /(GB/s)
GDDR5	~28GB/s	~400GB/s		0.9X of DDR3
Wide-IO	100+GB/s	~1TB/s		0.3X of DDR3
Serial + Wide-IO	100+GB/s	~1TB/s		0.5X of DDR3

TSV in Memory application

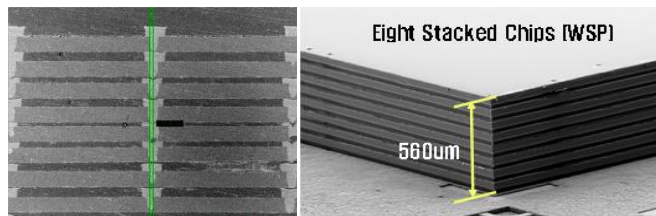
■ Can achieve more stacking & connection with thin profile

- More stacking → High density with less electronic loss
- More connection → Many IOs (Better performance)

Wire Bonding Type



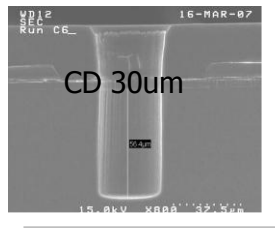
Thru Via Type



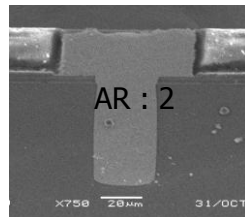
■ But it's high cost solution compared to wire-bonding

- Key bottleneck: Thin wafer/die handling (50um), Drilling/Filling/Align

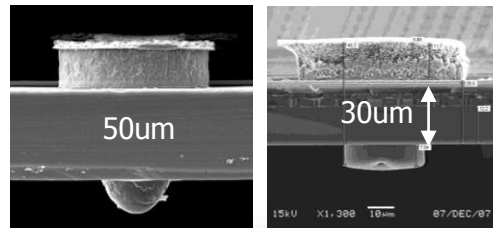
Via Machine



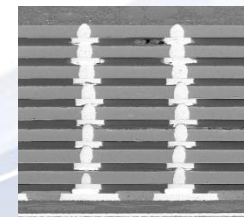
Filling



Thinning

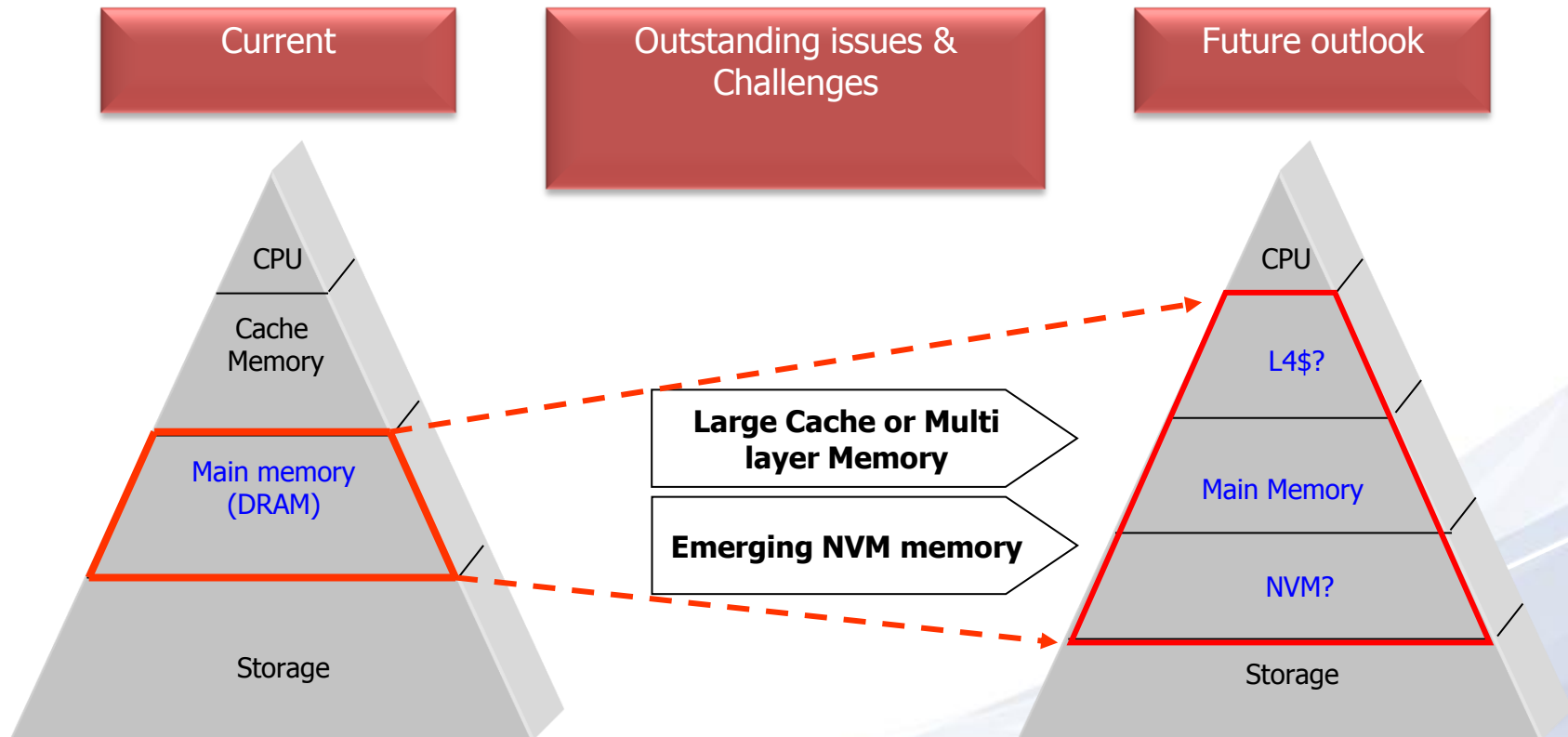


Bonding



**TSV technology is promising for future DRAM's capacity and performance increase
But, the issue of increased cost should be addressed**

■ Will the memory hierarchy still be the same?



Collaboration within End-User/Platform/CPU/Memory is Essential !

New Memory Cell structures are in development

Volatile Memory

SRAM

DRAM

Non-Volatile Memory

Charge Trap

NAND

NOR

Charge-Based Device

Resistance Change

PRAM

RRAM

STT-MRAM



Phase-dependent Resistance changes

Interface or bulk Resistance changes

Magneto-Resistance changes

Resistance-Based Device

Resistance change memory cells are good candidates due to DRAM compatible cell size, latency, & power

On active research for these to find new memory solution

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- **HPC is vision of future Server/PC, so Close Collaboration among End User/System/Platform level is highly important**
- **Memory in HPC has developed in evolutionary steps.**
 - DDR1 → DDR2 → DDR3 → ...
- **However, future of HPC Memory will face new challenges**
 - Whole memory hierarchy including storage may need to change
 - Samsung invites to a dialogue and active collaboration to jointly create the next evolutionary steps and prepare for a possible paradigm shift

Summary

- 1 Samsung = sustainable leading edge technology**
- 2 Today's excellence in mass production:
30nm class, DDR3, 32GB based on 4Gb**
- 3 Tomorrow's cutting edge:
 $\leq 20\text{nm}$, DDR4, DDR5 ... and TSV**
- 4 The day after tomorrow:
„Giga-investments“ + disruptive system memory technology**
- 5 The future is not to be predicted. Let's create it together!**

You can plant SAMSUNG Green Memory on your solution



www.samsung.com/greenmemory