Energy Aware Memory Technology and New Memory System Hierarchy

2013. 09

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Waking up from long lethargy

What we know today

- So far: when new technology was on starting block, next generation technology was in design phase: Future was clear

![Graph showing the development, market adoption, and obsolescence of various technologies over time. The graph includes timelines for SDRAM, DDR, DDR2, DDR3, and DDR4, with key years marked such as 1990, 1997, 2002, 2005, 2009, and 2016.](image)

*Highest speed in that year.*
Waking up from long lethargy

What will come next?

- Scenario 1: Business as usual → DDR5
Waking up from long lethargy

What will come next?

- Scenario 2: Virtually nothing

[Graph showing the development, market adoption, and obsolescence of different generations of DRAM technologies from 1990 to 2016. The graph includes markers for RDRAM, SDRAM, DDR, DDR2, DDR3, and DDR4.]

*Highest speed in that year.
Waking up from long lethargy

What will come next?

- Scenario 3: Evolutionary steps in back-end process to win time

Scenario 2: Extended DDR4 lifetime

Scenario 3: Scenario 2 plus performance uplift through 3D back-end technology

[Diagram showing the timeline of development, market adoption, and obsolescence for various memory technologies from 1990 to 2016.]

*Highest speed in that year.
Waking up from long lethargy

- Scenario 4: Revolutionary step

*Highest speed in that year

- Development
- Market adoption
- Obsolescence (in IT)
1. DRAM Technology

2. NAND Flash Technology

3. Large Capacity System Memory
Scaling approaches a physical limitation

- Technology difficulties & large investment

[Graph showing DRAM scaling with Technology Node (nm) on the x-axis and various performance metrics (Performance, Retention Time, Power, Density, Bandwidth) on the y-axis, indicating a trend towards limitations with progression.]
Memory Wall

The performance gap between required and offered is ever-increasing

- Disruptive approach is required to overcome
Memory Hierarchy Consideration

How to fit into the requirements of performance, capacity, power and etc.

- Role assignment by purpose

1. Channel count limitation
2. Max speed limitation
   - Parallel interface
   - Multi-drop
   - Single-ended I/O

Future

1. High-Bandwidth Memory (HBM)
   - Bandwidth driven
   - Latency advantage
2. Large Capacity Memory (LCM)
   - Capacity driven
   - Non-volatility

1. High B/W Memory
2. Large Capacity Memory
## Candidates for High-Bandwidth Memory

### HBM (High-Bandwidth Memory) vs. HMC (Hybrid Memory Cube)

<table>
<thead>
<tr>
<th></th>
<th>HBM</th>
<th>HMC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PKG type</strong></td>
<td>MPG A(Micro Pillar Grid Array)</td>
<td>BGA</td>
</tr>
<tr>
<td><strong>Logic function</strong></td>
<td>Buffer / Rerouting</td>
<td>Memory controller, SERDES</td>
</tr>
<tr>
<td><strong>CMD protocol</strong></td>
<td>Deterministic</td>
<td>Non-deterministic</td>
</tr>
<tr>
<td><strong>Max. bandwidth</strong></td>
<td>128~256GB/s</td>
<td>4link: ~160GB/s, 8link: ~320GB/s</td>
</tr>
<tr>
<td><em><em>Power</em> / Chip size</em>*</td>
<td>1X / 1X</td>
<td>1X(USR**) / 1.1X</td>
</tr>
<tr>
<td><strong>Capacity per cube</strong></td>
<td>2/4GB</td>
<td>2/4/8GB</td>
</tr>
<tr>
<td><strong># of bank</strong></td>
<td>~128banks (@4GB)</td>
<td>~512banks (@8GB)</td>
</tr>
<tr>
<td><strong>Capacity extension</strong></td>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
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</tbody>
</table>

*Assume IDD4R condition

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**Si Interposer**

![Diagram](image)

**CPU**

![Diagram](image)

**X1K IO**

![Diagram](image)

**Host**

![Diagram](image)

**HBM**

![Diagram](image)

**HMC**

![Diagram](image)

**Ultra Short Reach**
Contents

1. DRAM Technology
2. NAND Flash Technology
3. Large Capacity System Memory
History of Samsung NAND Flash

- Keep the technology leadership through continuous scaling
  - Worldwide No.1 market share in NAND Flash since 2002

- Scaling is getting difficult
  - Need a technical breakthrough to continue after sub-1ynm

- 120nm 1Gb
- 90nm 2Gb
- 70nm 4Gb
- 60nm 8Gb
- 50nm 16Gb
- 40nm 32Gb
- 1ynm 128Gb

- 1999
- 2003
- 2006
- 2013
Floating Gate Technology

- The number of stored electrons and error threshold reduce
  - Cell-to-cell interference is another barrier to move smaller nodes

![Graph showing number of stored electrons and error threshold over design rules from 120nm to 12nm.](image)
Technology Breakthrough for NAND

- Less costly technology and relaxed design rule
- Reduce coupling noise by structural changes

2D Planer NAND

Widen the gap by structure change

3D-NAND

SSL Gate
Control Gate(W/L)
GSL Gate
CSL

Poly Channel
ONO
Poly channel
CTF dielectrics
Metal gate

n+ n+ n+
**VNAND (Vertical NAND)**

**VNAND is a good successor of planar NAND**
- VNAND can continue to shrink less than effective 1ynm
- VNAND can keep offering higher density with more shrinks

<table>
<thead>
<tr>
<th>Cell Architecture</th>
<th>Planar NAND</th>
<th>VNAND</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Horizontal View" /></td>
<td><img src="image" alt="Vertical View" /></td>
<td></td>
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</tbody>
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<table>
<thead>
<tr>
<th>Advantages</th>
<th>Easy to produce with simple process</th>
<th>High reliability &amp; process reuse</th>
</tr>
</thead>
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<tr>
<td>Challenges</td>
<td>Shrinking under sub-10nm</td>
<td>Stacking</td>
</tr>
</tbody>
</table>
Contents

1. DRAM Technology
2. NAND Flash Technology
3. Large Capacity System Memory
Large Capacity System Memory

- Integrated solution to provide the large capacity system memory
  - Utilizing NAND flash memory
  - Solution technology (controller, firmware, and host S/W) should be engaged
Basic Configuration

- Large capacity system memory utilizing NAND flash
  - Improved host S/W response time
  - Data persistency and low power by non-volatile feature
NAND Flash As System Memory

**Generic solution for storage-class memory (SCM)**
- Less tight binding to the conventional interfaces
- Alternative SCM approach utilizing fast NAND
- The controller of LCM opens up new functions

![Diagram]

**Fast NAND**
- Low READ & WRITE latency
- Lower cost
- More scalable with VNAND

**PCIe SSD as another bulk and fast storage, or memory expansion**
- Easy adoption and expansion with an unified interface standard
- Enhanced random and sequential performance by reducing latency and enabling high levels of parallelism
Recently Released Products

Samsung Starts Mass Producing Industry’s First 3D Vertical NAND Flash

SEOUl, Korea – August 6, 2013 – Samsung Electronics Co., Ltd., the world leader in advanced memory technology, today announced that it has begun mass producing the industry’s first three-dimensional (3D) Vertical NAND (V-NAND) flash memory, which breaks through the current scaling limit for existing NAND flash technology.

“By applying our 3D V-NAND ... Samsung is providing its global customers with high density and exceptional reliability, as well as an over 20 percent performance increase and an over 40 percent improvement in power consumption,”

SEOUL, Korea – July 18, 2013 – Samsung Electronics Co., Ltd., the world leader in advanced memory technology, today announced that it has developed the industry’s first 2.5-inch (SFF-8639) NVM Express* (NVMe) PCIe solid state drive (SSD) to open up the high-end enterprise storage market.

Samsung Now Mass Producing Industry’s Most Advanced DDR4, Using 20 Nanometer-class Process Technology

The 4Gb-based DDR4 has the fastest DRAM data transmission rate of 2,667 megabits per second – a 1.25-fold increase over 20nm-class DDR3, while lowering power consumption by more than 30 percent.
Summary

- Disruptive approaches are required to overcome the DRAM challenges
  - High-Bandwidth Memory
  - Large Capacity Memory

- VNAND can prolong the NAND flash scaling

- NVM utilization to enable large capacity system memory
  - Combine the advantages of each memory type, and overcome the shortcomings
  - Solution (integration) technology is a key to success
Thank you